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CMOS Gate Array Characterization Procedures

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Present procedures are inadequate for characterizing the radiation hardness of gate array product lines prior to personalization because the selection of circuits to be used, from among all those available in the manufacturer's circuit library, is usually uncontrolled. (Some circuits are fundamentally more radiation resistant than others.) In such cases, differences in hardness can result between different designs of the same logic function. Hardness also varies because many gate arrays feature large custom-designed megacells (e.g., microprocessors and random access memories—μPs and RAMs). As a result, different product lines cannot be compared equally. A characterization strategy is needed, along with standardized test vehicle(s), methodology, and conditions, so that users can make informed judgments on which gate arrays are best suited for their needs.

The program we describe developed preferred procedures for the radiation characterization of gate arrays, including a gate array evaluation test vehicle, featuring a "canary" circuit, designed to define the speed versus hardness envelope of the gate array. A multiplier was chosen for this role, and a baseline multiplier architecture is suggested that could be incorporated into an existing standard evaluation circuit chip.

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1. Introduction

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The program we describe developed preferred procedures for the radiation characterization of gate arrays, including a gate array evaluation (GAE) test vehicle, featuring a "canary" circuit, designed to define the speed versus hardness envelope of the gate array. A multiplier was chosen for this role, and a baseline multiplier architecture is suggested that could be incorporated into an existing standard evaluation circuit (SEC) chip.

This program addresses the following question, originally posed by the sponsoring organization:

> *There is no industry standard method for characterizing the ionizing dose response of gate arrays. Can we produce one that will thereby provide an objective basis for comparing gate array hardness between vendors?*

Recent trends in the strategies of parts procurement have deemphasized screening as the chief means of assuring quality and hardness in favor of an approach based on establishing design and manufacturing disciplines that assure the quality of parts. This approach culminated in the quality manfacturers list (QML) program, which qualifies a manufacturing line, not merely individual components produced on a line. (Both electrical quality and radiation hardness can be controlled under the QML program.) If one attempts to apply this approach to gate array products, however, one sees that a major factor in the ultimate hardness of integrated circuits is at present uncontrolled—that is, the choice of the circuit library elements that will be used. This feature of gate arrays makes them different from other integrated circuits in how they must be characterized for radiation response.

The gate array product was developed to allow the user a quicker and less expensive way to implement his logic designs in silicon than is possible using custom design approaches. The user, rather than a designer who resides at the factory, decides how his function is to be realized. The user is provided with a basic matrix of simple gates, a library of predesigned functions implemented with these gates, and, in some cases, a set of custom-designed macros that can be readily inserted into the matrix to invoke functions not easily achieved in the gate array format (e.g., RAMs, ROMs,* μPs, etc). Such a set of choices means that it is unavoidable for the user to be presented with the opportunity to select some circuits that are more or less radiation-hard than others. In other words, given the same logic function to implement, different users produce personalizations that differ, both electrically and from a radiation hardness point of view. How, then, can one characterize the hardness of a gate array product line, when that hardness is so dependent on the user, over whom there is little or no control? Must systems treat each personalization as a new product, and recharacterize it for radiation response? If so, then a major advantage of gate arrays over custom designs is negated, and the concept of line qualification suffers. This is the conundrum facing those who would characterize the radiation hardness of a gate array product line, and it is the problem addressed under this program.

2. Technical Approach

Gate arrays are sometimes characterized for radiation hardness by testing of actual product circuits—sometimes test chips. Some manufacturers prefer characterizations of the actual chip, believing that this is the best yardstick of product hardness. Unfortunately, this approach is contrary to that underlying the concept of line qualification.

The use of product chips for radiation evaluation requires that additional samples of each circuit be manufactured merely for testing purposes, which increases testing costs significantly for the types of devices being discussed. The alternate approach, based on the use of test chips, would permit hardness validation of processes, and is presently being done as a part of the QML program. It offers the advantage of permitting quality assurance of lines with a minimum of product testing. It also permits comparison testing of different manufacturer's product offerings, and therefore is of great value to prospective users. However, no basis exists to assure that the test

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Read-only memories.

chips selected are representative of the product chips which might be built.

Many test chips have been proposed, including macro circuits (building block circuits implemented in the gate array) and test vehicles such as those used under the QML program or MIL-M-38510/ 605A (technology characterization vehicles, parametric monitors, process monitors, and SECs). The standard benchmark sets (such as Joint Electronic Devices Engineering Council (JEDEC) Standards 12 and 12-2) have also been suggested, but little quantitative data exist to support their selection over other candidates.

Both the test circuit and the product circuit approaches suffer from a lack of a widely accepted method for rating the quality of a test, so the choice cannot presently be made on a quantitative basis. This program is attempting to determine whether such a basis exists, and, if so, what it might be.

The approach used to address this problem consisted of six tasks:

- Determine what methods had been used previously to characterize the radiation hardness of gate arrays;

- Consider what test vehicles should be used in the characterization of gate arrays;

- Identify critical test conditions which should be standardized, and evaluate the implications of adopting preferred procedures for these conditions;

- Identify recommended tactics for the logic testing of gate arrays for use in radiation environments, namely, state initialization, clocking, bias conditions, etc;

- Identify recommended tactics to be used in parametric testing, e.g., how to determine I_{DD} (a personalization-specific parameter); and

- Based on the results of these tasks, develop a set of preferred procedures for the radiation testing and characterization of gate arrays for use in military systems.

2.1 Characterization Procedures Currently In Use

2.1.1 LSI Logic

LSI Logic Corp. has developed a strategy [1] for radiation characterization of their LRH10000 radiation-hard gate array family which is

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based on the use of ARACOR X-ray exposure for radiation-hard process development and as a hardness assurance test at the wafer level. They expose both test transistors on each wafer and a chip called a radiation-hard evaluation device (LRH10038Q) during the process development phase, and they use test transistors as process control monitors (PCMs). They specify the performance of their circuits at total dose levels well below those at which the devices "fail" (the specification level is 1 Mrad, while the failure level is well beyond this level), so they feel confident using this strategy.

The LRH10038Q has several macrofunctions which are intended to show potential users the power of this product line. The circuits available on the chip consist of a 16 × 16 multiplier, a 128 × 8 RAM, a 512 × 16 ROM, a number of delay characterization cells (ring oscillators with various amounts of loading), and some common medium-scale integrated (MSI) logic elements such as an 8 to 3 priority encoder, a 4-bit arithmetic logic unit (ALU), a 4-bit up/down counter, an 8-bit bi-directional shift register, a 9-bit parity generator, and an 8-bit magnitude comparator. Gate delays for the ring oscillators and access delays for some macros were measured versus total dose to characterize the process, and could be used as PCMs, if desired by the customer.

LSI Corp. was sensitive to the problem of users who might undertake the unrestricted design of gate arrays, thus resulting in circuits of varying total dose hardness. Since they service a broad range of clients, LSI experts admit that some might choose library elements selected for performance only, with a concomitant degradation in hardness. They see no obvious way to prevent this, without curtailing the marketability of the product line.

2.1.2 Harris Semiconductor Corp.

Harris uses the same radiation hardness assurance strategy for both their complementary metal-oxide semiconductor/silicon on sapphire (CMOS/SOS) and their bulk CMOS gate array product lines. They have characterized both product lines for hardness using a test chip called a radiation-hard demonstration vehicle (RHDV). This circuit consists of a number of macrocells, including a shift register, a pseudo-random number generator, a 4-bit ALU, an RS flip-flop, a 101-stage ring oscillator, a 1K × 1 bit RAM, and a 256 × 1 ROM. Samples of each chip were drawn from different wafers in a single manufacturing lot, and exposed to total doses up to 1 Mrads(Si) (three samples) and 10 Mrads(Si) (two samples). I_{DD} and stage delays were measured versus temperature, voltage, and total dose. Based on the results of these tests, Harris personnel conclude that

both product lines are functional to 10 Mrads(Si), that leakage changes occur for both types of product, with CMOS/SOS being much more sensitive in this regard, and that speed is little affected by radiation. They prefer to use either product chips or this test device as a hardness assurance tool, rather than test chips containing individual components. Quality Conformance Inspection requires the use of a product chip.

2.1.3 Honeywell Corp.

In their characterization of the RICMOS-3 gate arrays, Honeywell uses a plan based on ARACOR testing of process monitor bars on all wafers, and of two SRAMs per wafer from three different wafers in each lot. They do not think it is possible, at present, to perform product acceptance testing for radiation-hard parts based on test chip data alone, unless large margins exist and safe circuit design techniques have been used, since test chips accentuate shifts, while digital circuits are designed to be tolerant of such conditions as parameter shifts.

2.1.4 United Technologies Microelectronics Corp. (UTMC)

In characterizing their gate array products, UTMC uses the JEDEC 12-2 set, a reliability test chip, a technology test chip, and a product engineering test chip (featuring long chains and other specialized features). They characterize cells independently of one another and perform exhaustive testing of each such cell, so that the problem of testing vary-large-scale integrated (VLSI) chips using these cells is alleviated. They compare test results from the standard test devices with their data sheets and design simulation results for all AC and DC specifications. All key categories of cells in the design library are included in the standard test device, and must be evaluated under varying fan-outs. Typical categories include flip-flops, NAND, NOR, and inverter cells. UTMC also pointed out the need to evaluate rebound and/or low-dose-rate total-dose effects. All the circuits in their cell library are designed to optimize hardness, so they do not see a problem in unrestricted design by users. They do not anticipate any possible design that would result in a part softer than their own designers would produce.

UTMC, along with the other manufacturers who were queried, emphasized the importance of standardizing characterization procedures in such a way that SEU response could be carried in a compatible fashion, and preferably on the same test chip. UTMC suggested that the SEU characterization be done not only with RAM cells but also with registers, using the "worst-case" register in the cell library,

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if known. If the worst-case register is not known, then all available registers should be included.

2.2 Selection of Test Vehicle

Strategies for hardness characterization of CMOS gate arrays may call for the use either of a product circuit or of a test chip as the test vehicle. The use of product circuits is risky since one cannot be assured that simply because a specific design is successfully hardened all other designs of that gate array will be successful. Unfortunately, the use of a test chip results in an even more serious shortcoming—that the successful demonstration of the hardness of a test chip does not necessarily demonstrate the hardness of *any* personalizations of that gate array. Quality specialists have faced a similar problem in developing test vehicles for use in line qualification under the QML and Qualified Parts List (QPL) programs and, in response, have developed the concept of a SEC chip, to serve as a test chip (see also app A for comparison). The SEC chip, therefore, is the first choice to be investigated for possible use as a test vehicle for the hardness characterization of gate arrays.

To extend qualification of a gate array product line on the basis of SEC testing, it is imperative that the product circuits be manufactured "identically [2]" with the SEC. Since "identity" is incapable of demonstration, especially as it relates to radiation hardness, some ambiguity exists here. One interpretation says that qualification should be extended if "worst-case" design guidelines have been used in designing the SEC. Characterization of a gate array necessarily means characterization of its library of circuits, since circuit selection plays such a major role in determining the hardness of gate array personalizations. Therefore, worst-case design guidelines must be applied in the selection of circuits for use on the SEC. At present, there is no agreement on how this should be done, and the ambiguity is unresolved. Thus, the SEC chip does not satisfy the need for a test chip for gate array evaluation. Other candidates must be considered.

Two criteria can be established for the selection of circuits to be included in the GAE for gate arrays:

- The radiation-induced failure modes to which personalizations may be subject must be identified and evaluated in the radiation testing of the GAE.

- The set of circuits used should include subcircuits that are representative, not only of the SSI/MSI* functions contained in the library, but also of the large macros found in many gate array libraries, such

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*SSI/MSI: Small-scale integrated/medium-scale integrated.

as RAMs, ROMs, etc. (These are often custom designs, and thus pose unique problems.)

There have been various suggestions for the makeup of the gate array evaluation chip. We review the principal ones and recommend which approach best justifies extending the qualification to future personalizations.

2.2.1 JEDEC Standard Benchmark Sets

The sets of benchmark circuits identified in JEDEC Standard 12 (*Standard for Gate Array Benchmark Set*) and Standard 12-2 (*Standard for Cell-Based Integrated Circuit Benchmark Set*) were prime candidates for the role of test vehicles for radiation characterization of gate arrays. Tables 1 and 2 list these circuits and the reasons for which they were included in the standards.

Table 1. JEDEC Standard 12: Standard for Gate Array Benchmark Set.

Benchmark circuit	Purpose	TTL equivalent
4-bit ALU	Tests cost/efficiency of typical MSI ALU function.	74S381
16-bit ALU	Tests cost/efficiency of typical MSI ALU function.	74S381
4-bit rotator	Tests ability to implement complex logic; tests routing density.	N/A
16-bit rotator	Tests ability to implement complex logic; tests routing density.	N/A
8-bit register	Tests flip-flop speed and density.	74S374
8-bit up/down counter	Tests counter performance.	N/A
3-8 decoder	Tests ability to implement simple combinational logic.	74S138
16 x 4 RAM	Tests ability to implement complex sequential element; tests cost of memory.	74S189
9-bit parity generator	Tests ability to implement complex logic/routing.	74S280

Table 2. JEDEC Standard 12-2: Standard for Cell-Based IC Benchmark Set.*

Benchmark circuit	Purpose
256 x 4 and x 9 RAM	Test cost/efficiency of nibble and byte (plus parity) wide memory functions.
16 x 4 ROM Patch	Tests cost/efficiency of small ROM used for logic patch purposes and programmed at interconnect level.
2K x 4 and x 9 ROM	Tests cost/efficiency of program ROM programmed either at the diffusion or interconnect level.
Small and large PLAs	Tests cost/efficiency of programmable logic array (PLA) capability.
2:1 Analog MUX	Tests cost/efficiency of simple analog circuit.
Comparator	Tests cost/efficiency of moderately complex analog function.
8-bit D/A converter	Tests cost/efficiency of complex analog function.

*TTL equivalents are given, since with the exception of the RAMs (similar to the 2101, the circuits listed in the table have no equivalents among TTLs.

Standard No. 12 has as its purpose the provision of a common set of high-level functions that serve as vehicles for comparing the performance of gate arrays implemented in any technology using any internal structure. These benchmarks were intended to provide an unbiased measure of a gate array vendor's ability to implement a desired complex function on a particular gate array at a known level of performance. Standard 12-2 was intended to provide the estimated performance of some commonly used MSI functions which might be found in a cell-based technology.

A close examination of both sets, however, shows that they do not provide a good measure of gate array radiation hardness. First, the circuits were not chosen with any consideration for radiation-induced failure modes and consequently do not tell a user what he can expect from his design, unless he uses only these same circuits. Also, since their adoption as standards, the state of the art has advanced considerably, with the result that they do not provide sufficient information for today's users. For example, many modern gate arrays offer macros which are, in reality, VLSI in their own right, not merely implementations of TTL* SSI/MSI. JEDEC committee JC-44 (the committee that originated Standard 12-2) agrees with this assessment. They believe the standard to be obsolete, even for their purposes, and they may rewrite and reissue it. As a result, the use of JEDEC 12 and JEDEC 12-2 benchmark circuit sets for gate array hardness evaluation is not recommended, and a test chip better suited to the evaluation of gate array hardness is needed.

2.2.2 Other Benchmark Sets

Commercial Benchmarks.—Other approaches to a benchmark for the GAE chip were also considered. Table 3 shows one alternative benchmark set, proposed [3] for an evaluation of commercial gate

Table 3. Proposed commercial benchmark for gate array evaluation.

Function	Purpose	Gate count	TTL equivalent
3–8 decoder	Simple combinational logic	20	74138
8-bit register	Flip-flop speed and density	40	74374
16-bit barrel shifter	Complex logic/ routing density	300	—
16x4 RAM	Complex sequential element and cost of memory	350	74189
3-state bi-directional pad	Driver efficiency	5*	—

*Number of internal gates. Also requires large buffer and one or more pads.

*TTL: transistor-transistor logic.

arrays carried out at the same time as development of the JEDEC benchmark set, but better suited to actual gate array applications than the JEDEC set. Unfortunately, this set does not take into account the radiation-induced failure modes either, and therefore suffers from the main shortcoming of the JEDEC sets. Also, in today's technological environment, the macros proposed are much too small to exercise the very large arrays now available.

Microprocessor Chip Sets as Benchmarks.—Microprocessor chip set circuits were suggested for possible use as benchmarks. Two circuit families in particular were of interest: the SA3000 family from Sandia Laboratories and the general processor unit (GPU) chip set developed by the Air Force Materials Laboratory. Table 4 shows which chips are in the Sandia set and provides a general description of the function of each chip. Detailed information on these chips could not, however, be obtained. Apparently, no final report on the SA3000 chip set development effort was ever written, and the available information is insufficient to permit it to be used as a standard without significant design activity on the part of each vendor.

Information was obtained on the GPU chip set [4,5] that describes in detail the function of each chip. Table 5 gives the electrical and physical properties of this chip set. Block diagrams for each chip, and detailed logic diagrams of the GP001 were obtained, but information on the other chips was minimal, so they could not be used as a set for the GAE chip, either. GP503, however, is attractive as one element of a GAE chip, as described in the following paragraphs.

Optimum Benchmark Set for Test Vehicle.—An approach has been identified that corrects the shortcomings of the above-mentioned

Table 4. SA3000 chip set.

Part No.	Function	Transistors	Pins
SA3000	8-bit CPU, logic emulation of Intel 8085	18,000	40
SA3001	256×8 SRAM with timer (Intel 8155/56)	17,700	40
SA3002	2K×8 ROM (Intel 8355)	20,700	40

Table 5. GPU chip set.

Part No.	Function	Gates	Pins
GP001	8-bit slice processor	?	48
GP301/302	512×8/256×16 ROM	?	28
GP501	Emulating controller	?	48
GP502	12-bit microprogram sequencer (AM2910)	?	40
GP503	Asynchronous, concatenatable 8×8 two's complement multiplier	?	64
GP504	Address select unit	450 gates	48
GP505	Register select unit	450 gates	48
GP507	Interrupt control unit	450 gate	48
CMM5104	4K×1 static RAM	?	24

benchmark sets. It would use some of the JEDEC circuits, chosen to provide radiation test data on commonly used SSI/MSI functions, combined with a "canary" function that would be chosen to exercise the dominant radiation-induced failure modes. The former circuits would represent the maximum hardness that could be achieved with the array. The latter circuit would be selected to demonstrate radiation-sensitive performance such as that resulting from a design optimizing speed at the expense of hardness.

Figure 1 shows a block diagram of the proposed test chip (the GAE chip) intended for use in the total-dose response characterization of CMOS gate arrays. The random logic block contains selected circuits from JEDEC standards (12 and 12-2). In addition to random logic, however, the test chip must accommodate megacells, large macros, etc. This will be done through a bus-oriented architecture that permits the inclusion of drop-in functions, if such are available, but does not mandate them.

As seen in figure 1, blocks as varied as memory, μPs, A/Ds, and Muxes can be included. A 16-bit data bus and an 8-bit address bus should be adequate to support such a mix. A three-level clock generation and distribution network (CDN) has also been added that will permit the evaluation of total dose damage on clock skew in the fast circuits now becoming available. This architectural concept is compatible with JEDEC Standard 12-5 (Design for Testability Guidelines), and should be completely testable using the scan techniques of Standard 12-5, obviating concerns about incomplete fault coverage of the test chip.

Six SSI/MSI-level functions and one input/output (I/O) pad have been included in the random logic block shown in figure 1. Table 6 lists these circuits. Data on these circuits, combined with data from

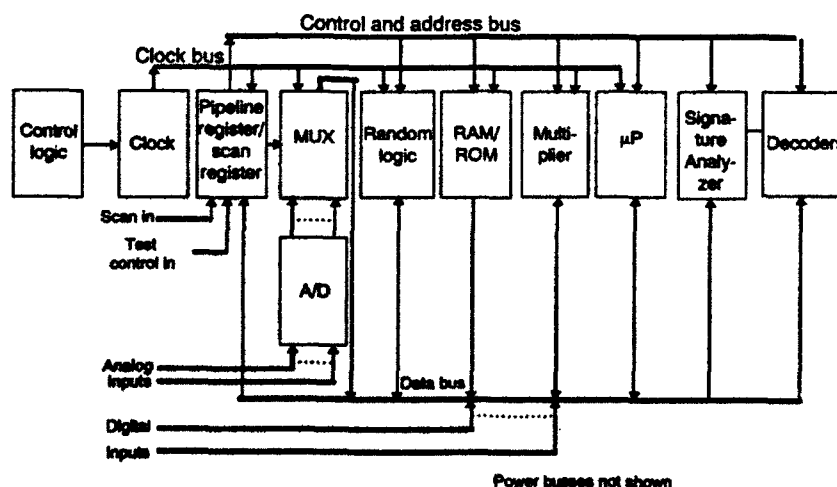**Figure 1. Block diagram of GAE chip functions.**

Power busses not shown

Table 6. Proposed random logic circuit for use in GAE chip.

Benchmark circuit	Purpose	TTL equivalent
16-bit ALU	Tests cost/efficiency of typical MSI ALU function.	74381
16-bit rotator	Tests ability to implement complex logic; Tests routing density.	—
16-bit register	Tests flip-flop speed and density.	74175
16-bit up/down counter	Tests counter performance; used in clock circuits.	74193
4-16 decoder	Tests ability to implement simple combinational logic.	74154
16-bit parity generator	Tests ability to implement complex logic/routing.	74S280
3-state bi-directional pad	Tests driver efficiency/ hardness.	—

process monitor chips, will permit the hardness of well-designed chips to be determined, and will therefore serve to provide a "best-case" estimate of the hardness of the gate array product line.

Clocking and timing uncertainties in digital systems are becoming a major concern as clock rates increase and cycle times shorten. Many high-frequency microprocessors require a nearly perfect 50-percent duty cycle for their input clock signal. The high frequency of these signals makes the clock input specifications very demanding. For example, the Intel 50-MHz i486 requires a clock period of 20 ns, and if a clock skew as small as 1 ns occurs, functional failure might result. The speed of the μP would suffer if the on-chip clock distribution network (CDN) were to degrade due to radiation exposure, so that a difference of 1 ns was introduced into the branch of the clock tree feeding one side of the chip relative to that of the clock tree feeding the other side. Such problems are new to the hardness assurance community, and their potential impact will have to be studied carefully. Addition of a CDN would permit the evaluation of this radiation-induced failure mechanism for gate arrays.

For some users and some product lines, total-dose characterization requires the study of an assortment of megacells, such as RAMs, ROMs, μPs, Muxes, and A/Ds. The bus-oriented architecture proposed will accommodate such circuits, as seen in figure 1.

The inputs to the pipeline register/scan register shown in figure 1 contain both scan-in and test control signals. These are the only two additional testing signals required. The outputs of this register consist of control and address signals connected to the control and address bus, data signals connected to the data bus, and a control signal connected to the multiplexer for the A/D converters. The pri-

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mary input/primary output and the primary input (PI) lines are directly accessible from outside the circuit. The pipeline register/scan register serves the dual purpose of a conventional pipeline register during normal operation and a scan-in register during testing. The multiplexer for the A/D converters may consist of transmission gates. The other two blocks are the signature analyzer and the decoders.

The hardware overhead of this technique is reflected in the signature analyzer, decoders, and modifications that make the pipeline register serve a dual purpose. Only one signature analyzer is needed, since it can serve each of the other blocks. However, a separate decoder is needed for each block.

The characterization of the total-dose hardness of a gate array requires the use of a test vehicle that properly represents the hardness that will be achieved with future personalizations of the array. Unless the manufacturer's library of circuits is tightly controlled, users can select circuits or logic elements that are not the optimum choice from a hardness point of view. Thus, characterization based only upon the hardest circuits in the library is not representative.

One candidate for use as the test vehicle for gate array characterization is the SEC chip, used under the QML and QPL programs. Careful consideration has shown, however, that the SEC chip is not a good choice for this purpose. Under both the QML* and QPL systems, the manufacturer is free to define his own SEC chip. In view of this, he would be foolish to design one which is anything but super-hard. Yet users may not have the same latitude when dealing with real system requirements. They will be asked to achieve performance levels that make their systems competitive with other systems. Therefore, hardness levels obtained on the SEC bear no relationship to what they will achieve. For this reason, gate arrays cannot be accurately characterized using the SEC. Rather, a chip is needed that fairly represents what users will experience in realistic, performance-driven applications. The GAE chip defined in this report attempts to achieve this objective.

The GAE chip we propose would contain, in addition to others, a circuit selected to demonstrate the magnitude of the radiation-induced degradation that can be expected in designs where performance (speed) is emphasized at the expense of hardness. Such a circuit is referred to as a canary, and the proper choice of this circuit

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*The decision to let the manufacturer select the SEC was made with the expectation that he would choose the circuit he was producing in greatest numbers. This assumption does not apply to gate arrays, yet the use of the SEC to control qualification-extension persists, to the detriment of gate array quality.

is extremely important to the characteization of gate array products. It is the presence of a canary circuit on the GAE chip that permits it to describe the worst-case hardness level achievable with the gate array. (The best-case is described by the total-dose performance of the random logic block of circuits.) This provides an even-handed assessment of overall product hardness, and makes the proposed GAE superior to other SECs in establishing the criterion on which qualification-extension will be based.

After much study, it was decided that a high-speed digital multiplier (16×16 or larger) meets the requirements of a canary circuit. Digital multipliers can be implemented in a number of variations [6–10]. The one that best exercises total-dose damage mechanisms in the pursuit of speed should be selected from among the many available designs. The metric to be used would be the VHSIC metric of "thru-put," as measured in gates-Hz/cm^2. By providing information on both the thru-put of the test circuit and its radiation hardness, characterization data on the canary circuit would show prospective users what they could reasonably expect in their use of the array. The canary circuit would not be a "dumb" design, but one chosen to define a realistic point on the hardness versus performance envelope of the array. To motivate the vendors to participate in the characterization activity, the mechanism for extending radiation-hard qualification of gate arrays should be changed. Vendors whose canary circuit proved to be hard to a level D_1 would be granted automatic qualification extension for parts having a total-dose specification less than D_1, while vendors whose canary circuit proved hard to a level D_2 (where $D_1 > D_2$) would only be able to claim automatic qualification extension to the lower level. This circuit is further described in section 2.6.

2.3   Test Conditions

As stated in section 2, task 3 of this program required the identification of critical test conditions that should be standardized as well as evaluation of the implications of adopting preferred procedures for these conditions. The strategy outlined in the discussion of test chip definition (sect. 2.2.2) is one that isolates the dominant radiation-induced failure mechanisms by selecting circuits that are prone to these mechanisms and tests them in such a way as to facilitate their observation. Thus, the principal "critical test condition" calls for the incorporation of both hard circuits and those which demonstrate radiation-induced failures. (Previous approaches would exclude such "soft" circuits.) The careful selection of a canary circuit accomplishes the latter objective. This circuit is then tested in a way that observes

the failures produced, using both digital testing techniques and parametric testing techniques chosen to identify specific nodes sensitive to specific failures.

2.3.1 Digital Testing

The digital testing approach is attractive since ICs can suffer from either parametric or functional (digital) radiation-induced failure modes. The former type of tests can be performed on standardized test circuits, and the resultant data can be applied to all ICs built with the same process, or tests can be performed on the product chip itself. However, performing such testing on a standardized test chip offers the advantage of permitting hardness characterization of processes (just as the QML procedure permits quality assurance of lines with a minimum of product testing). It would also permit comparison testing of different manufacturer's product offerings, and therefore would be of great value to prospective users.

Functional (digital) testing, however, is product specific, and cannot be done in a representative fashion on anything but an actual product chip. Furthermore, functional testing has, to date, not been quantifiable except by testing the entire function of the chip, which requires large numbers of quite expensive devices. Thus, the value of digital testing in helping assess product hardness has been minimal. Since there seems no alternative to some use of product chips in a gate array characterization program, the hardness assurance community faces the challenge of devising a method of assessing functional hardness in a cost-effective way, and in a manner that can be quantified. The possible use of logical testing to determine the total-dose level at which the first radiation-induced faults appear in product chips offers a number of advantages:

- Minimal cost impact, since test vectors for "stuck-at" fault testing are always generated during chip design, and they typically offer high node coverage.

- No special equipment required, since this is a basic element in IC production, and many testers offer this capability.

- Quantifiable, since many circuit blocks are used to sensitize a given node and then propagate its response to a primary output. A metric exists for assessing the quality of a chip, based on the node coverage provided by stuck-at fault testing [11]. According to this metric, the fraction of bad chips accepted, DL, is

$$DL = 1 - Y^{(1-T)} ,$$
(1)

where

DL = defect level,

Y = yield (fraction of chips which are good after radiation),

and

T = fault coverage.

To illustrate the defect levels which this equation predicts, if a sample of nine product chips were subjected to hardness assurance total-dose testing, and no faults were observed after X rads(Si), the yield could be said to be greater than 90 percent ($Y \geq 0.9$). If these chips were subjected to stuck-at testing providing node coverage of 0.9, 0.95, 0.99, and 0.999, the fraction of bad chips that could be claimed are predicted to be <0.0105, 0.0053, 0.0011, and 0.000105. Thus, one can trade off sample size for node coverage and achieve the same quality level. Such an approach offers advantages when chips are more expensive than testing.

As a further illustration, one sees that if 100-percent node coverage is achieved, the equation would predict a zero defect level. The implications of extrapolating to this extreme must be examined carefully before exaggerated claims are made, but it is an intriguing example of what could be achieved in hardness assurance by designing chips to be testable, so that 100-percent stuck-at fault coverage is achieved.

Unfortunately, digital testing also has some disadvantages in a hardness program. First, the stuck-at fault testing is based on an assumption that there is only a single fault in an otherwise perfect chip. Once radiation-induced faults begin to appear (as the total dose to which a sample of chips is being exposed is increased), multiple faults will doubtless appear, and the entire approach would be expected to fail, since the node being interrogated by a given test vector set may produce a fault signal that is masked by other faults in either the sensitization path or the propagation path. Also, radiation-induced faults may not show up when test vectors are applied at the low rates typically used for stuck-at fault testing, but would degrade performance when the chip is run at maximum rate. I_{DDQ} testing may offer an alternative approach free from some of these problems, and will be addressed in our next report.

Section 2.4 details the tactics that accomplish these objectives for digital testing. The implications of adopting this approach to gate array characterization include specifying certain types of test equipment. A detailed discussion of test equipment for VLSI is beyond the scope of this effort, but some facets of it are presented below to direct the efforts of those interested in pursuing the topic.

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If recommended procedures are adopted for digital testing of irradiated ICs, one implication would be increased testing costs. Digital testers can be expensive. To minimize the cost impact, it is necessary to understand the different types of testers available. The main classes of general-purpose automatic test equipment (ATE) available for digital testing of CMOS gate arrays are as follows:

- *Stored results type*—In this type of test machine, both the stimulus pattern and the anticipated response pattern are stored in the machine. The response pattern could have been derived from a simulation; also, some machines have the capability of "learning" the response pattern from a known good circuit. Costs increase with memory size.

- *Comparison testers*—Here the response to the test is not pre-stored. Instead, the outputs of the circuit under test are compared with those from a "golden standard" circuit to which the tests are being applied simultaneously. This type is less expensive than the Stored Results type.

- *Random testers*—In random testers, the input sequence is not pre-stored. Instead, the tester can generate a sequence of pseudorandom inputs to the circuit and to a golden standard. Often the response is measured in terms of transition counts on the various nodes of the circuit, because the test sequences are too long to allow the storing of detailed results. Again, the cost of memory is saved.

- *System testers*—In this type, the circuit is plugged into a working prototype of the system for which it is being designed. Such testing is the preferred approach for speed testing, but it lacks diagnostic flexibility, and has no means of objective determination of test value (e.g., fault coverage).

2.3.2 Parametric Testing

Parametric testing attempts to detect faults affecting the magnitude of a circuit parameter (but not the logic). Parametric testing of LSI circuits does not differ substantially from that of SSI/MSI—the testing task increases proportionally with the number of pins on the chip package. Radiation-hard LSI circuits tend to fail as a result of parameter degradation due to radiation exposure, so parametric testing would be the preferred strategy for such components. The big question is exactly what kind of parametric testing should be done. Packaged-part parametric tests include DC and AC tests. DC tests include shorts, opens, maximum current, leakage, output drive current, and threshold levels. AC tests include propagation delay,

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setup and hold, functional speed, access time, refresh and pause time, and rise and fall time. Radiation testing of VLSI circuits has concentrated on this type of testing. It does not differ substantially from that done on SSI/MSI—the testing task increases linearly with the number of I/O pins on the chip. Since the pin count increases much less than linearly with the gate count, it consumes a smaller and smaller portion of total system testing costs as chip complexity grows. Further, it is a type of testing with which the technical community is familiar. Thus, as long as parametric failures remain the dominant radiation-induced failure mode, existing methods are adequate to characterize CMOS gate arrays, and it is only necessary to define a standardized test circuit and standardized procedures for such a characterization to proceed. If radiation-induced functional failures begin to pose a problem, then not only is a standardized test chip needed, but new methods also have to be developed.

I_{DDQ} testing [12] is a new type of parametric testing that has received a great deal of attention recently, and which seems to hold promise for use in radiation characterization because of its diagnostic capabilities.

In a CMOS device in the quiescent state, all the internal logic levels have settled to a steady-state value. If the device is healthy, the I_{DDQ} being drawn by the MOSFETs is very low. (For a CMOS IC operating from a 5-V rail, I_{DDQ} is about 10 nA.) When the logic levels are changing, the paired N- and P-channel transistors are simultaneously turned on. This creates a momentary low-impedance path through the device and, together with the current required to charge and discharge any parasitic capacitances, causes the transition current (I_{DDT}) to be hundreds of milliamperes. This provides a method for parametrically testing logic nodes that are buried deep within complex CMOS ICs, using far fewer test vectors than for conventional logic-response functional testing or digital logic testing.

To understand how the reduction in test vectors occurs, consider the fact that a conventional digital test must sensitize the node in question, toggle it to produce the proper (or faulted) signal, and then propagate this signal to a primary output pin of the DUT before it can be detected. If the fault occurs at a node that is nested deep within the logic of the DUT, a very long stream of vectors is required to sense the condition, and another long stream to carry the information on the existence of the fault to the output for detection. To test with the I_{DDQ} method, it is only necessary to sensitize the node, and then switch it to logic 1 and to logic 0 while measuring the current drain. One assumes observability by monitoring the supply current,

thereby eliminating the need for the vectors used to propagate the fault signal to the output.

On the plus side, I_{DDQ} testing is particularly effective in the detection of transistor "stuck-on" faults, which is one of the radiation-induced faults expected in CMOS technology. (N-channel transistors that are driven from enhancement mode to depletion mode by total dose would appear to be stuck-on, and would therefore be detected.) On the minus side, I_{DDQ} testing is limited in the rate at which vectors can be applied. The requirement for measuring the currents after the transients have settled imposes a limit on the maximum data rate at which I_{DDQ} can be measured. The only VLSI tester having a hardware A/D that permits I_{DDQ} measurements at high speed is the Advantest T3342 with the bit current option. Several testers that permit monitoring of I_{DDQ} are the HP 82000 and 83000, the Schlumberger STS9000 and Sentry 20 and 21, the Trillium, the Teradyne, and the Tektronix.

2.4   Recommended Tactics for Logic Testing of Gate Arrays

The optimum tactics for use in radiation characterization of gate arrays are those which best elucidate the worst-case failure mechanisms that users can anticipate, without conjuring up a worst case that is unreasonably severe. Important considerations are clock speeds, logic loading, bias conditions, test vector sets, and state initialization procedures.

2.4.1   Recommended Clock Rates

A radiation-induced failure mechanism of great interest to users of modern gate arrays is that occurring as a result of degradation of drive currents. This exhibits itself in the form of logic errors at high clock speeds. Functional testing at 1 MHz does not detect these errors efficiently. To assure that characterization data address these concerns, it is necessary that the clock speed at which the GAE chip is tested be the highest speed at which the product line is likely to be used. Since this is not known with accuracy for gate arrays when the product line is initially being characterized, it is necessary to examine what relationship has been found to exist between system cycle time and gate propagation time of logic ICs, and to test at the lowest likely cycle time (highest clock frequency).

Studies [13] have shown that the average switching period (T_S) in high-speed systems is related to the elemental circuit propagation delay, t_{sd}, of the logic stages:

$$T_S = kt_{sd} \, , \tag{2}$$

where k = switching factor.

In this equation, T_S is closely related to the machine cycle time whereas t_{sd} is related to the basic circuit delay as shown below:

$$t_{sd} = t_{do} + \Delta t_d C_{in} f_o + \Delta t_d C_W \, , \tag{3}$$

where t_{do} is the inherent circuit propagation delay,

$\quad\quad\quad C_{in}$ is the input capacitance of the driven stage,

$\quad\quad\quad \Delta t_d$ is the delay per unit load capacitance,

$\quad\quad\quad f_o$ is the fanout, and

$\quad\quad\quad C_W$ is the wiring capacitance.

The cycle time at which the gate array should be characterized is then given by k times the gate propagation delay exhibited by the technology. The value of k depends solely on the logical structure of the system, as long as the performance of the circuit is fully utilized within it. Designs that produce low values of k are superior to those with higher values. Fully pipelined systems achieve values of k as low as 4, but this is an extreme case. Conventional mainframe systems achieve values of k from 20 to 80 whereas minicomputer systems have values of k up to 200. In military applications, the methods used to harden CMOS circuits usually consist of techniques that will increase k, thereby reducing the performance of the technology even further. However, there are no data available on what values of k are obtained with actual hardened systems. Therefore, there is no choice but to characterize arrays at the high clock frequencies representative of a low value of k. From the definition, k is related to the operating frequency of the chips as shown below:

$$f = 1/(2\,kt_{sd}) \, . \tag{4}$$

Using the lowest value cited by Masaki [13], it is recommended that the clock frequency used be that for $k = 20$.

2.4.2 Recommended Loading

To determine f from equation (4), we must specify the loading conditions under which t_{sd} should be determined. Equation (3) shows that t_{sd} consists of three terms: the intrinsic gate delay, the time to charge the input capacitance of the next stage(s), and the time to charge the line capacitance. It is reasonable to specify that each of these terms

would be equal in an optimally designed system, so that the clock frequency should be calculated using the relationship

$$f = \frac{1}{(2\,kt_{sd})} = \frac{1}{(6\,kt_{d0})} \,.$$ (5)

Thus, the clock frequency at which the gate array should be evaluated is the reciprocal of 120 times the inherent gate delay of the gate array. For a technology featuring gates with an intrinsic delay of 0.5 ns, this would require a clock frequency of 16.67 MHz. As technology advances occur which permit higher speed operation, this frequency will rise, and testing will have to be done at even higher speeds.

2.4.3 Recommended Bias Conditions

In view of the wide range of applications for which gate arrays can be used, the characterization process should gather as much data as possible to permit users to extract the information needed for their systems. For this reason, clocked circuits should measure minimum and maximum functional frequencies versus total dose as a function of supply voltage, for supply voltages up to V_{DD} + 10 percent (V_{DD} = 5.5 V for a 5-V nominal system). Decreases in maximum functional frequency are usually due to the negative shift difference between PMOS threshold voltage and NMOS threshold voltage. Minimum supply voltage increase is usually due to PMOS threshold voltage negative shift.

2.4.4 Recommended Test Vector Sets

Determination of the worst-case test vector set for logic testing depends on the failure mechanisms anticipated in the critical path. While an enormous amount of work has been done studying the failure modes at the basic device level, much less has been done in determining the radiation-induced failure modes of ICs. In view of the role that circuit design can play in determining failure modes, a "bottoms-up" approach (inferring chip failure modes from device response) is uncertain at best, especially for the very large chips of interest today. Therefore, the technical literature was searched for studies that attempted to determine IC failure modes. Several classes of studies have been done: One determines experimentally the radiation failure levels of specific commercial chips [14,15]; another attempts to relate the radiation response of hardened chips to the radiation response of component devices [16,17]; and yet another attempts to apply a "top-down" approach (predicting chip failure modes from logic level analysis [18–21]). The approach that seems

best suited to determining the worst-case test vectors for the many elements of the GAE chip is that originally proposed by Bhuva [18], which uses simple, rule-based calculations to identify vulnerable subcircuits and worst-case irradiation and operating conditions. Consequently, this is the method recommended for determining the test vector set for gate array characterization.

2.4.5 Recommended State Initialization Procedures

The architecture proposed for the GAE chip has been designed in accordance with JEDEC Standard 12-5 (*Design for Testability Guidelines*), and should be completely testable using the Scan techniques of Standard 12-5, obviating concerns about state initialization procedures and incomplete fault coverage of the test chip.

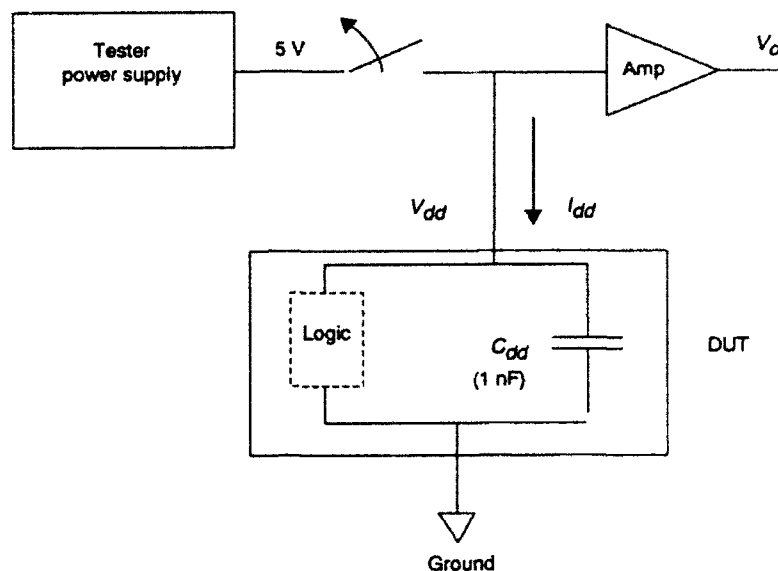## 2.5 Recommended Tactics for Parametric Testing of Gate Arrays

Parametric testing of integrated circuits has been the preferred method since the inception of the integrated circuit industry. In general, the tactics for measuring these circuits are well developed and require no further clarification for testing the GAE chip. Testers are reminded, however, that CMOS/TTL buffers are always a point of concern when studying the total-dose sensitivity of ICs, and care should be taken when evaluating the parametric changes that take place in these circuits due to radiation.

One relatively new aspect of parametric testing where innovative tactics are needed is that of I_{DDQ} testing. As shown previously (sect. 2.3.1), this technique, while a parametric test, requires the generation of digital test vectors to access the node whose parameters are to be tested. Thus, the procedures recommended in section 2.4.4 are recommended for generating the vector to be used. Once these vectors are available, the basic circuit used to measure I_{DDQ} is that proposed by Keating [10], and shown in figure 2.

2.6 Preferred Procedure for Gate Array Characterization

Preferred procedures for the total-dose hardness characterization of CMOS gate arrays should be applicable to both commercial product offerings and to military products, hardened and unhardened. The procedures recommended as a result of the work done under this program specify use of a GAE chip (which would be irradiated in accordance with MIL-STD-883D, Test Method 1019.4), and tested as discussed in sections 2.3, 2.4, and 2.5 of this report. The GAE in-

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Figure 2. Keating circuit.

Figure 2. Keating circuit.

cludes a circuit that exercises the important radiation-induced failure mechanisms, and verifies that, even for a very sensitive design, the gate array produces adequately hard parts.

A high-speed 16 × 16 multiplier (or larger) is recommended for the role of canary circuit on the GAE chip. The design details of this multiplier would be determined to exercise the important radiation damage mechanisms. (This circuit would not be a "dumb" design, but would be one chosen to define a realistic point on the hardness versus performance envelope of the gate array.) Such a circuit would provide a common basis for comparing the performance versus hardness capabilities of gate array product lines. The metric to be used would be the VHSIC metric of "thru-put," as measured in gates-Hz/cm^2. Product lines whose canary circuit proved to be hard to a level D_1 would be assumed to permit the design and fabrication of gate arrays hard to this level, while product lines whose canary circuit proved hard to a level D_2 (where $D_1 > D_2$) would only be able to claim product hardness to the lower level.

The circuit selected for use as a canary should meet the following requirements:

- It should be representative of the functions readily implemented in structured arrays (not RAM or ROM).

- It should be a useful circuit, so that the quality of the design can be assessed.

- It should exercise the important total-dose-induced failure mechanisms.

- It should be a circuit that can be implemented in various ways, so that design innovation can be permitted.

The function recommended for this purpose is the parallel multiplier. Such circuits are used extensively in μPs, where the multiplier function is the limiting factor in both the performance (speed) and die size of most μP chips today. They are also used in digital signal processors, floating-point units, etc., where they seem to be needed in ever-larger sizes, with single chip versions as large as 54 × 54 having been reported recently [7]. In most modern multiplier designs, the modified Booth algorithm [22] reduces the number of propagation stages with no significant penalties. The number of stages can be further reduced using a Wallace tree [23], but the wire lengths can become long, and must be dealt with carefully in designing large, fast multipliers.

Other design approaches to multipliers include array multipliers. An array-type multiplier consists of an array of units with full adders and partial-product bit generators, where each of the units processes single-bit data consecutively. Such a circuit can be regularly laid out with only a few unit cells, making the design easy, but the resultant products are too slow for high-speed systems. These considerations make the design of parallel multipliers a challenge to VLSI designers, and numerous papers have been published recently dealing with this topic. Data are available on the speed and power (but not the hardness) of various designs, most of which fall into the area of the delay versus power space shown in figure 3.

Since multiplier designs emphasize speed and efficient use of silicon area, and use such subcircuits as OR/NOR logic, full adders, and long wire runs, they are also expected to exhibit many of the important radiation-induced failure mechanisms. Therefore, there will be a trade-off between speed and hardness, which is one of the requirements for the circuit to be used as the canary. We met the goal of this program by identifying the need for a canary circuit, and recommending the use of a digital multiplier for this purpose. It is recommended that, as a followup to this program, the various design approaches to the multiplier function be explored so that one can be selected to be used on the GAE chip, and that the GAE chip be implemented in one or more gate array product lines to demonstrate its utility in the characterization of the radiation hardness of CMOS gate arrays.

Figure 3. Delay versus power, CMOS 16-bit multipliers.
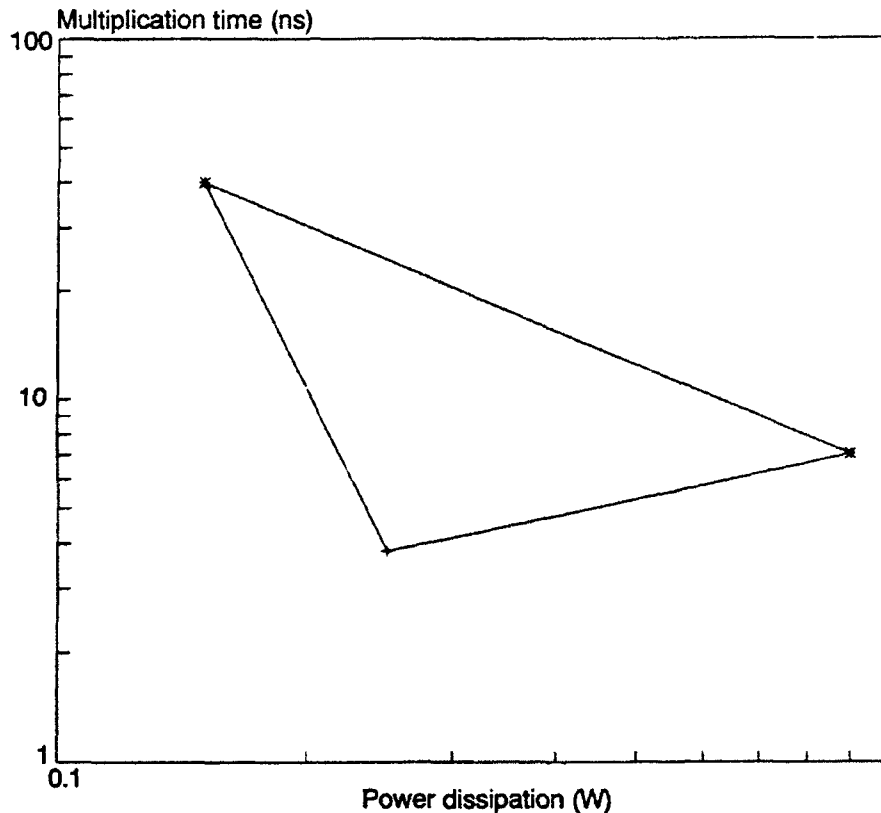
3. Conclusions and Recommendations

3.1 Conclusions

Procedures used for characterizing the radiation hardness of gate array product lines prior to personalization are makeshift and/or inadequate. These shortcomings arise due to the fact that the selection of circuits used in gate arrays and, in some cases, even the circuit design, are uncontrolled. Suppliers of radiation-hard gate arrays usually design their library circuits to be hard to total-dose effects, but libraries often contain several circuits that can perform the same function, and hardness differences may exist between these different options. When selection of circuits is left to the user, as it often is with gate arrays, differences in hardness can result for the same logic function. (Fig. 4 illustrates the lack of control over logic and circuit design in military parts.)

Another source of hardness variability is seen when we realize that many gate array product lines feature large, custom-designed mega-cells (e.g., μPs, RAMs, etc.). Commercial suppliers do not observe radiation-hard design guidelines, but are driven by performance and/or cost considerations only. (There is little information in the literature as to what

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ASIC type	Fabrication process	Manufacturing rules	Design rules
Gate array	FAB Certified line	Tools	Circuit/ logical design rules
Standard cell	SPC		Hardness design rules
Full custom	Process monitor die	☐ = Covered	

constitutes radiation-hard circuit design. Appendix B presents a brief summary of radiation-hard design guidelines that should be observed in CMOS circuits.) As a result, the hardness that can be expected from actual product gate arrays can easily be overstated by enthusiastic vendors, and an even-handed comparison of different vendor's products is problematical. A characterization strategy is needed, along with standardized test vehicle(s), methodology, and conditions, so that system users can make informed judgments on which product lines are best suited for their needs.

These standardized procedures should satisfy the following requirements.

• They should be accurate: Characterization data must describe the hardness that users can expect to realize in the applications to within a factor of no more than three, so that hardness assurance design margins can be estimated before fabrication.

• They should have diagnostic value: Users should be able to identify those circuit library elements that impact product hardness, so that alternate approaches can be considered.

• They should be compatible with the two different approaches to line qualification of gate arrays (QPL* and QML).

• They should be inexpensive; i.e., they should not require many parts, and the costs should be allocatable to the product lines which require radiation hardness, and not spread over all product lines.

While this report was in preparation, Defense Electronics Support Center (DESC) announced that they were merging the QPL program with the QML program. However, since those products already being supplied under the QPL program will be "grandfathered" into the new combined system, the comments made here are still applicable.

3.2   Recommendations

This program developed recommendations for preferred procedures for the radiation-characterization of gate arrays. The approach recommended uses the GAE chip specified in section 2.2.2, including the canary function discussed in section 2.6.1. To implement these recommendations, additional work needs to be done to optimize the specific design to be used for the digital multiplier canary circuit. In the meantime, the canary circuit described in appendix C is suggested as a baseline multiplier design, which could be incorporated into existing SECs. The slice characteristic of this design facilitates scaling it to be representative with the gate count in the array being characterized.

The strategies used to test the GAE chips should combine functional testing with conventional parametric testing. The functional testing used should employ the tactics specified in sections 2.3 and 2.4 in selecting the clock rates, loading, bias conditions, and state initialization procedures. The test vector sets used should be the sets developed by the designer for design verification, augmented by those vectors selected using the procedures described in section 2.4.4 to identify radiation-sensitive nodes. Advanced digital and parametric (I_{DDQ}) testing (sect. 2.3.1) could be used, at the discretion of the vendor, to gather diagnostic data on radiation-induced failure mechanisms and node coverage information not otherwise available.

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Appendix A. Qualification of Radiation-Hard Gate Arrays

Preferred procedures for the total-dose hardness characterization of complementary metal-oxide semiconductor (CMOS) gate arrays must be applicable to both commercial product offerings and to military products, hardened and unhardened. However, the problem of total-dose characterization of gate arrays from military suppliers, especially JAN qualified parts list (QPL) and qualified manufacturers list (QML) lines is of special interest, and is used below to provide a scenario against which the workings of the preferred procedure proposed above can be assessed.

Under present procedures, a gate array product line can be certified under either the JAN QPL system, or the QML system, although the QML system was clearly not designed with gate array products in mind. Table A-1 summarizes the features of these systems. The qualification process requires qualifying one standard evaluation chip (SEC), for JAN QPL lines, and one SEC chip and two product chips for QML lines. Current QPL documentation states that, in view of the controls that exist over the manufacturing process, qualification extension to lower gate count arrays is automatic, provided that the parts are manufactured "identically." This raises the question of how to determine whether the parts have been manufactured identically.

Differences of opinion exist about how qualification should be extended to other personalizations of an array, once the SEC is qualified. One school says that each personalization should be treated as a new product and qualified exactly as the SEC was. The second school of thought holds that once the SEC has been qualified, quali-

Table A-1. Gate array quality system comparison.*

Feature	JAN QPL	QML
Customer requirements	Altered item drawing	Standard military drawing
Change control	DESC approval	Manufacture's TRB
Design system certification	Required	Required
CAD verification test chip	JEDEC benchmark circuits	Manufacturer's design
SPC	Required	Required
TCV test chip	Not required	Required
SEC test chip	Required	Required
Elimination of screening tests	Yes	Yes
Alternate nondestructive pull test	Allowed	Allowed
Qualification	One SEC required	3 lots of SEC 2 lots of product
Red·.ced QCI testing	Reduced sample size	Allowed per TRB
Faul coverage	95 percent	99 percent

*L. DeBacker, *Comparison of JAN QPL Gate Array Program to Other Military Quality Systems*, Johari Inc. (June 1992).

fication extension to new personalizations should be automatic, provided computer simulations show that the radiation hardness satisfies the specification.

The procedures recommended as a result of the work done under this program are based on a third position, which holds that qualification extension should be automatic, provided the gate array evaluation (GAE) chip shows a hardness level for the "canary" chip exceeding the total-dose specification of the personalization in question. This requires that the qualifying agency play a role in defining the SEC chip, and that the GAE chip identified herein be used for this purpose. The GAE includes a circuit that exercises the important radiation-induced failure mechanisms, and verifies that, even for a very sensitive design, the gate array produces adequately hard parts.

A high-speed 16×16 multiplier (or larger) is recommended for the role of canary circuit on the GAE chip. The design details of this multiplier would be determined to exercise the important radiation damage mechanisms. (This circuit would not be a "dumb" design, but would be one chosen to define a realistic point on the hardness versus performance envelope of the gate array.) Such a circuit would provide a common basis for comparing the performance versus hardness capabilities of gate array product lines. The metric to be used would be the VHSIC metric of "thru-put," as measured in gates-Hz/cm^2. Vendors whose canary circuit proved hard to a level D_1 would be granted automatic qualification extension for parts having a total-dose specification less than D_1, while vendors whose canary circuit proved hard to a level D_2 ($D_2 < D_1$) would only be able to claim automatic qualification extension to the lower level.

By means of this approach, the extension of line certification to individual personalizations, which is presently based on the properties of a vendor-defined SEC chip, would be based on the performance of a chip designed to illustrate not only the "best-case" hardness performance of the gate array, but also its radiation-sensitive characteristics.

Appendix B. Radiation-Hard Design Guidelines

A major consideration in defining the gate-array evaluation (GAE) chip is the set of radiation-hard design guidelines to be used. As stated previously, there has been little research on radiation-hard circuit design, and the existing literature is largely anecdotal. The guidelines that are available are summarized below:

- Eliminate dynamic circuitry.

- Use synchronous circuitry.

- Limit permitted fanout.

- Prevent clock skew problems by distributing clock signals on metal, avoiding cascading clock lines, using large on-chip clock buffers, etc.

- Restrict the height of stacks (e.g., limit the number of inputs permitted in NOR gates).

- Avoid the use of transmission gates.

To understand the impact of observing these rules, we need to consider complementary metal-oxide semiconductor (CMOS) design strategies and how they are affected by radiation-hard requirements.

Standard CMOS can be designed to make optimal use of silicon area, or to match rise and fall times. Most commercial gate array vendors optimize transistor sizes for area, consistent with the constraint that because most interconnections represent a fairly heavy load, the transistors should be large. Therefore, the widths and effective lengths of both NMOS and PMOS transistors are made identical. Because the pre-radiation mobilities of PMOS and NMOS transistors differ, the rise time of simple inverters is somewhat longer than the fall time. Series or parallel transistor connections affect the ratio of t_f to t_r. A two-input NAND gate would have nearly symmetrical switching characteristics (two series NMOS transistors "compensate" for the mobility difference) while a two-input NOR gate has $t_r = 4\ t_f$. (The series PMOS transistors compound the mobility difference.) Radiation-hard gate array vendors, on the other hand, would be expected to anticipate this loss in PMOS drive, and would size the N- and P-devices differently.

We can make rise and fall times symmetrical by adjusting the transistor sizes to compensate for the mobility difference. Where $\mu_n = 2\ \mu_p$, an inverter would be designed such that $W_p = 2\ W_n$. Equalizing rise and fall times by width adjustment provides the additional ben-

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efit of placing the inverter switching point at $V_{DD}/2$, thus providing maximum noise immunity (a benefit when designing for SEU tolerance). Because the widths have been sized to compensate for the difference in NMOS and PMOS mobility, the current is balanced when $V_{in} = V_{out} = V_{DD}/2$. Varying the ratio of W_p to W_n causes the switching point of a CMOS inverter to vary, just as varying the depletion/enhancement ratio changes the characteristics of an NMOS inverter.

A major problem that can be traced to this sizing difference occurs with the simple transistor-transistor logic (TTL)-CMOS level shifter: The PMOS transistor required to set the switching point to about 1.4 V and keep the DC current at an acceptable level leads to a very slow rise time for the level shifter. This exhibits itself in the fact that DC power is nonzero for TTL-compatible inputs. Because the desired switching point is so near the NMOS threshold, radiation-induced shifts in the NMOS threshold can be very deleterious. Thus, radiation-hard design guidelines must note the sensitivity of TTL-compatible inputs to radiation degradation.

CMOS transmission gates are often found to be sensitive to radiation-induced changes. Such gates are used extensively in latches and flip-flops to improve area and speed. They are superior to their NMOS counterparts in that they do not lose a threshold voltage near V_{DD} or ground. However, the additional inverter and the associated layout clearances cause the CMOS transmission gate to occupy more space than the NMOS pass transistor would. Stacked PMOS devices are also "bad actors" in a radiation environment, because large numbers of PMOS transistors in series can seriously degrade performance. For example, a 4-input NOR gate would have a four-fold degradation in rise time compared to an inverter.

Other design rules that could or should be imposed on gate array designs to enhance radiation hardness are the following:

- Wired-OR connections should be prohibited.

- Unused macro functions must be tied high or low.

- Delay-dependent logic functions (choppers, one-shot oscillators, etc.) should be prohibited.

- Observe Joint Electronic Device Engineering Council Standard 12-5, *Design for Testability Standards.*

Rule 1 implies that internal tri-state busses cannot be used, since internal floating nodes that might result can lead to incomplete switching and excessive power consumption, and can cause prob-

lems in initializing the circuit. Enforcing this rule would adversely impact the architecture of embedded microprocessors (μPs).

Rule 2 also addresses floating nodes.

Rule 3 addresses the difficulty in predicting the performance of circuits post-radiation when they use delay-dependent functions (Kim[1] addresses the problem of edge-triggered circuits in this regard).

Rule 4 ensures that the circuit can be tested, which is an important aspect of the hardness assurance problem.

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[1]W. S. Kim et al, *Radiation-Hard Design Principles Utilized in CMOS 8085 Microprocessor Family*, IEEE Trans. *Nucl. Sci. NS-30, 6 (December 1983), 4229–4234.*

# Appendix C. Baseline Design of Multiplier as "Canary" Circuit

The digital multiplier design recommended for use as a "canary" circuit is based on a design[1] developed for use in a CMOS bit-slice chip set, and the only one for which both design and radiation test data are available. While its original implementation was in a technology (6 μm) that today is obsolete, its architecture is still valid, and it should transfer directly into today's micrometer and submicrometer technologies. It is an asynchronous 8×8-bit concatenatable two's-complement multiplier, shown as a block diagram in figure C-1. The entire multiply operation occurs in a single microcycle. This circuit performs multiplication based on Booth's algorithm, two bits at a time. The multiplication technique for two's-complement numbers using the add and shift method is complicated by the correction step needed when the multiplier is negative. Much of this complication is eliminated in the Booth algorithm by treating positive and negative numbers uniformly, thereby eliminating the need for correcting the result.

As seen in figure C-1, two 8-bit operands, a and b (multiplicand and multiplier), are applied to the inputs, and their product ($c = ab$) appears at the output. A third 8-bit word may be applied to expansion inputs B to implement the function $c = ab + B$. All data inputs contain latches, so that when the input latch control signals are high, the respective input data are latched and will remain stable until a negative transition of the latch control occurs, at which time new data may be introduced. Four carry-in signals (CI 1-4) and four carry-out signals (CO 1-4) are provided to link with other chips to multiply larger words.

As seen in figure C-1, there are four identical adder stages in the multiplier. The function of each stage is controlled by three bits of the multiplier. Depending on the value of these bits, a multiple (0×, 1×, or 2×) of the multiplicand must be added to or subtracted from the product. These three bits of the multiplier are recorded into three control bits, two of which (PASS and SHIFT) control the generator of multiples. The generator of multiples can output zero, the value of the multiplicand (sign extended one bit), or the multiplicand shifted left one bit (using the value from b_{in} as the least significant bit (LSB)). The third recorded bit (COMPL) controls the complementer and internally generated carry-in. If COMPL is low, the complementer passes on the output of the generator of multiples unchanged. If

[1] K. Karstad, *Introducing and Applying the 8 × 8 CMOS/SOS Multiplier*, GP503, RCA *Application Note ICAN-7211*.

Figure C-1. Functional block diagram of 8-bit by 8-bit multiplier.
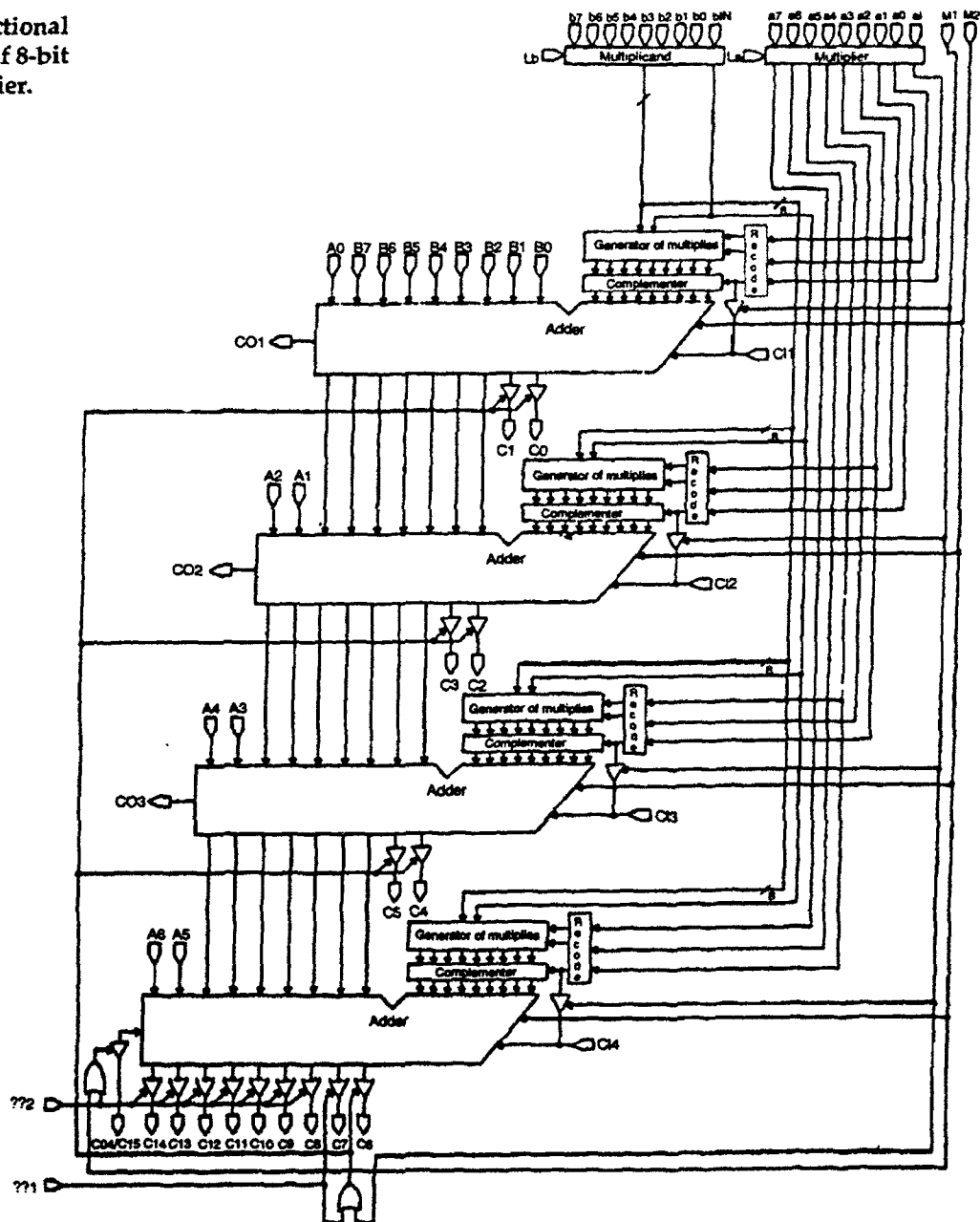
COMPL is high, the complementer complements the outputs of the generator of multiples.

When the multiplier is used in an array, the next two significant bits of the multiplicand and multiplier must also be available because of the requirements of Booth's algorithm. These bits are entered through pins a_{in} and b_{in}. At the least significant end of the operands, where no less significant bit exists, zero must be supplied to a_{in} and b_{in}. Thus, even though the circuit is an 8×8-bit multiplier, the operands are essentially nine bits wide.

The advantage of making the circuit concatenatable lies in the fact that one can combine basic cells to implement a multiplier for operands of arbitrary bit length by using more than one of these circuits. To achieve this feature, the circuit is configured so that it can be used in three ways, namely, "solo" (8- × 8-bit), concatenation (8n-bit × 8-bit), and cascading and concatenation (8n-bit × 8m-bit). To permit these modes, the circuit is controlled by mode control bits M1 and M2.

In the solo mode, in which the adders act as a 9th-bit extension of the 8-bit adders, the carry-in signals are internally generated, and the CI pins must be electrically free to float. The value of the MSB of the product appears at the output in this mode. Also, a_{in} and b_{in} are both set to zero. The carry-out signals, CO, are used to provide sign extension by connecting CO1 to expansion inputs.

The most significant slice mode is the same as the solo slice mode except that the carry-in input values are used as the carry-in values to the four adder stages. Inputs a_{in} and b_{in} are tied to the MSB inputs of the next less significant multiplier in the array.

In the least significant slice mode, the adders are transparent, leaving each adder stage as an 8-bit adder. The carry-in signals are internally generated. Inputs a_{in} and b_{in} are both set to zero. The expansion inputs are connected to the output pins of the next more significant multiplier in an array.

The middle slice mode is the same as the least significant slice mode, except for carry-in signals, which are used as the carry-in values to the adder stages. Inputs a_{in} and b_{in} are connected in the same way as in the most significant slice mode.

Karstad[1] reports that this multiplier architecture, when implemented in 6-μm CMOS/SOS (silicon on sapphire) and operated at 10 V, exhibited a 130-ns pre-radiation multiply time, and a 180-ns multiply time after exposure to 1 Mrad(Si). (Vendors fabricating it in today's gate arrays would be expected to obtain significantly better speed performance, as well as 5-V operation.) Since the details of the design of this circuit are intentionally left undefined (only the general architecture is specified), some vendors might implement it in a way that emphasizes speed at the expense of hardness, and might achieve, for example, 10-ns pre-radiation performance, with catastrophic part failure at 30 Krads(Si). Other vendors, using more conservative design principles, might achieve 20-ns pre-radiation per-

[1] K. Karstad, *Introducing and Applying the 8 × 8 CMOS/SOS Multiplier, GP503, RCA Application Note ICAN-7211.*

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formance, with part failure at 100 Krads(Si). Systems that need 10-ns multiply times must be prepared to survive with the reduced hardness. Those requiring high levels of hardness must be prepared to accept reduced speed. Users of gate arrays need access to the details of this performance/hardness tradeoff, if they are to make realistic comparisons of different product lines.

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